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A Comparative Analysis Of Different Topologies And Controls Of Multilevel Inverter

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Abstract
A multilevel inverter is a power electronic device that is widely applied in industries for high voltage and high power applications, with the added benefits of low switching stress and lower total harmonic distortion (THD), hence reducing the size and bulk of the passive filters. The paper proposes a new diode clamped multilevel inverter topology and comparative analysis of different topologies and controls of multilevel inverter . This paper showing the comparison between the three level and five level diode clamped multilevel inverter. Circuit configuration and theoretical operation also discussed in this paper. The performance of the topology is investigated through MATLAB-R2009a based simulation results.
Keywords-*Multilevel inverter, PWM Techniques, Total Harmonic Distortion.*

I. Introduction

Power electronic converters, especially dc/ac PWM inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, enhanced quality of product, better maintenance, and so on. For a medium voltage grid, it is troublesome to connect only one power semiconductor switches directly [1, 2, 3]. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations such as laminators, mills, conveyors, pumps, blowers, fans, compressors, and so on. As a cost able solution, multilevel converter not only obtain high power ratings, but also allow the use of low power application in renewable energy sources such as fuel cells, photovoltaic, and wind which can be easily interfaced to a multilevel converter system for a high power application.

The most frequent primary application of multilevel converters has been in traction, both in locomotives and track-side static converters [4]. More new applications have been for power system converters for VAR compensation and stability enhancement [5], active filtering [6], high-voltage motor drive [3], high-voltage dc transmission [7], and most newly for medium voltage induction motor variable speed drives [8]. Many multilevel converter applications focus on industrial medium-voltage motor drives [3, 9], utility interface for renewable energy systems [10], flexible AC transmission system (FACTS) [11], and traction drive systems [12]. The inverters in such application areas as stated above should be able to handle high voltage and large power. Therefore, two-level high-voltage and large-power inverters have been designed with
series connection of switching power devices such as gate-turn-off Thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors (IGBTs), because the series connection allows reaching much higher voltages. However, the series connection of switching power devices has big problems [13], namely, non equal distribution of applied device voltage across series-connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices during transient and steady-state switching operation of devices. As alternatives to effectively solve the above-mentioned problems, several circuit topologies of multilevel inverter and converter have been researched and utilized.

The output voltage of the multilevel inverter has many levels synthesized from several DC voltage sources. The quality of the output voltage is improved as the number of voltage levels increases, so the quantity of output filters can be decreased. Diode clamped inverter is the most commonly used

multilevel topology , in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Nabae, Takahashi, and Akagi were proposed neutral point converter in 1981 it was essentially a three-level diode-clamped inverter [14].

A. DIFFERENT TOPOLOGIES OF MULTILEVEL INVERTER

B. Cascaded H-bridge multilevel inverter

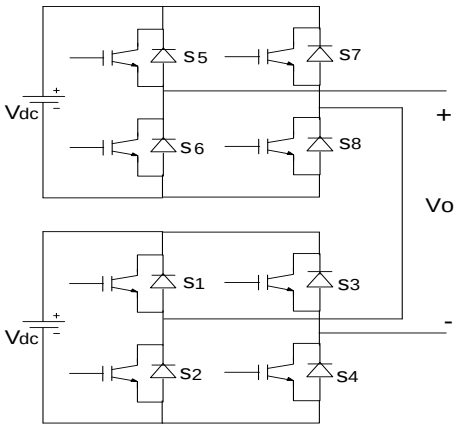

Fig.1. Cascaded H-bridge multilevel inverter circuit topology for 5- level inverter

The Cascaded Multi-level inverter was introduced by Hammond [15]. The series H-bridge inverter appeared in 1975. Cascaded multilevel inverter was not fully realized until two researchers, Lai and Peng. They patented it and presented its various advantages in 1997. Since then, the CMI has been utilized in a wide range of applications. With its modularity and flexibility, the CMI shows superiority in high-power applications, especially shunt and series connected FACTS controllers [16]. The CMI synthesizes its output nearly sinusoidal voltage waveforms by combining many isolated voltage levels. By adding more H-bridge converters, the amount of Var can simply increased without redesign the power stage, and build-in redundancy against individual H-bridge converter failure can be realized.

A series of single-phase full bridges makes up a phase for the inverter. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The converter topology is based on the series connection of single-phase inverters with separate dc sources. Figure 1 shows the power circuit for five-level cascaded inverter and it requires eight semiconductor switches, two dc sources of fixed values. Due to fixed dc value, it does not face the voltage balancing problem. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. This is made possible by connecting the capacitors sequentially to the ac side via the power switches. The resulting output ac voltage swings from -Vdc to +Vdc with three level, -2Vdc to +2Vdc with five-level.

C. Flying Capacitor Multilevel Inverter

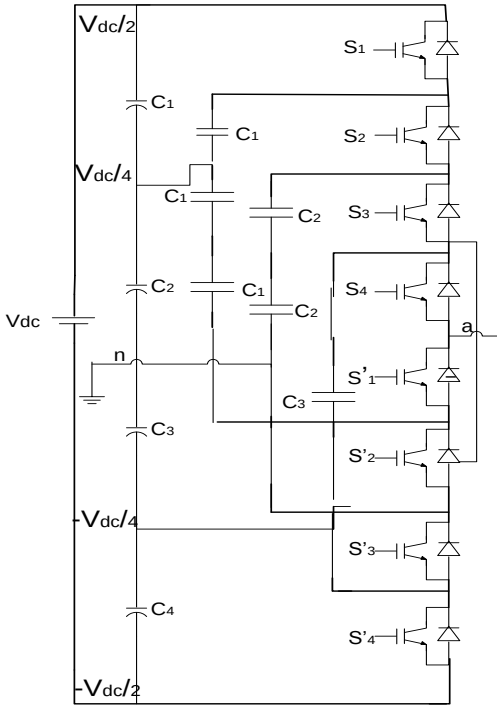

Fig.2. Flying Capacitor multilevel inverter circuit topology for 5- level inverter

The capacitor clamped inverter alternatively known as flying capacitor was proposed by Meynard and Foch. This is one of the alternative topology for the diode clamped inverter. The flying capacitor involves series connection of capacitor clamped switching cells. This topology has several unique and attractive features when compared to the diode-clamped inverter. One feature is that added clamping diodes are not needed. Furthermore, the flying capacitor inverter has switching redundancy within the phase, which can be used to balance the flying capacitors so that only one dc source is needed. Figure 2 shows the Five-level flying capacitor inverter.

II. PROPOSED TOPOLOGY

In this topology there are two pairs of switches and two diodes are consists in a three-level diode clamped inverter. All switch pair's works in complimentary mode and the diodes used to provide access to mid-point voltage. The DC bus voltage is dividing into three voltage levels with the help of two series connections of DC capacitors, C1 and C2. With

the help of the clamping diodes Dc1 and Dc2 the voltage stress across each switching device is partial to Vdc. It is supposed that the total dc link voltage is Vdc and mid point is synchronized at half of the dc link voltage, the voltage across each capacitor is Vdc/2 (Vc1=Vc2=Vdc/2). In a three level diode clamped inverter, there are three different feasible switching states which apply the stair case voltage on output voltage relating to DC link capacitor voltage rate. At any time a set of two switches is on for a three-level inverter, and in a five-level inverter, a set of four switches is on at any given time and so on. Switching states of the three levels inverter are summarized in table-1.

I. TABLE SWITCHING STATES IN ONE LEG OF THE THREE-LEVEL DIODE CLAMPED INVERTER

Switch Status	**State**	Pole Voltage
S1=ON,S2=ON S1'=OFF,S2′=OFF	S=+ve	$V_{ao}=V_{dc/2}$
S1=OFF,S2=ON S1'=ON,S2′=OFF	S=0	$V_{ao}=0$
S1=OFF,S2=OFF S1'=ON,S2′=ON	S=-ve	$V_{ao}=-V_{dc/2}$

Fig.3. shows a three-level diode-clamped converter in which the dc bus consists of two capacitors, C1 and C2. For dc-bus voltage Vdc, the voltage across each capacitor is Vdc/2 and each device voltage stress will be limited to one capacitor voltage level Vdc/2 through clamping diodes. To explicate how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point.

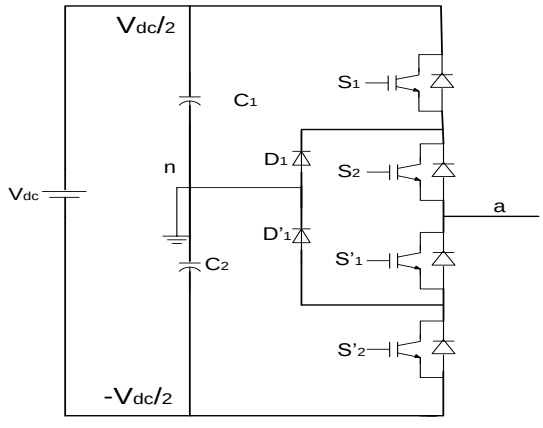

Fig.3.Three level diode clamp multi-level inverter

II. TABLE SWITCHING STATES IN ONE LEG OF THE FIVE-LEVEL DIODE CLAMPED INVERTER

Voltage V_{ao}	Switch state							
	S 1	***S 2***	***S 3***	***S 4***	***S 1'***	***S 2'***	***S 3'***	***S4 '***
$V_{ao}=V_{dc}$	1	1	1	1	0	0	0	0
$V_{ao}=V_{dc/2}$	0	1	1	1	1	0	0	0
$V_{ao}=0$	0	0	1	1	1	1	0	0
$V_{ao}=-V_{dc/2}$	0	0	0	1	1	1	1	0
$V_{ao}=-V_{dc}$	0	0	0	0	1	1	1	1

Fig.4. shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C2, C3, and C4. For dc-bus voltage V_{dc}, the voltage across all capacitor is $Vdc_{/4}$ and each device voltage stress will be limited to one capacitor voltage level $V_{dc/4}$ through clamping diodes.

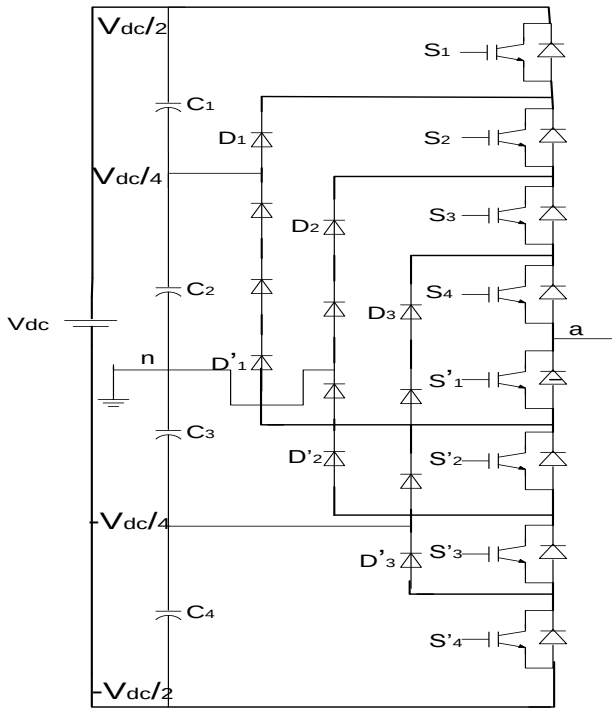

Fig.4. Five level diode clamp multi-level inverter

III. Modulation Techniques

Multilevel converters are mainly controlled with sinusoidal PWM extended to multiple carrier arrangements of two types: Level Shifted (LS-PWM), which includes Phase Disposition (PD-PWM), Phase Opposition Disposition (POD-PWM) and Alternative Phase Opposition Disposition (APOD-PWM) or they can be Phase Shifted (PS-PWM) [17]. In propose topology APOD is used.

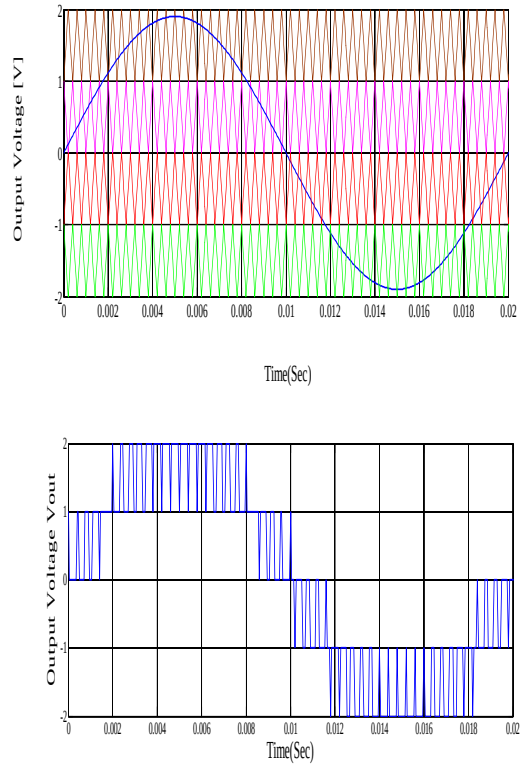

Fig. 5. Proposed modulation techniques (APOD) for five level multilevel inverter

IV. Simulation Results

In this paper, the simulation results of the 3-level and 5-level for the proposed multilevel inverter, using series- parallel switching multilevel dc-link inverter topology are simulated by MATLAB R2009a software module. The parameter of the simulation are as following R=2 ohms, C=4000e-6F, Frequency of carrier signal is 2 kHz.

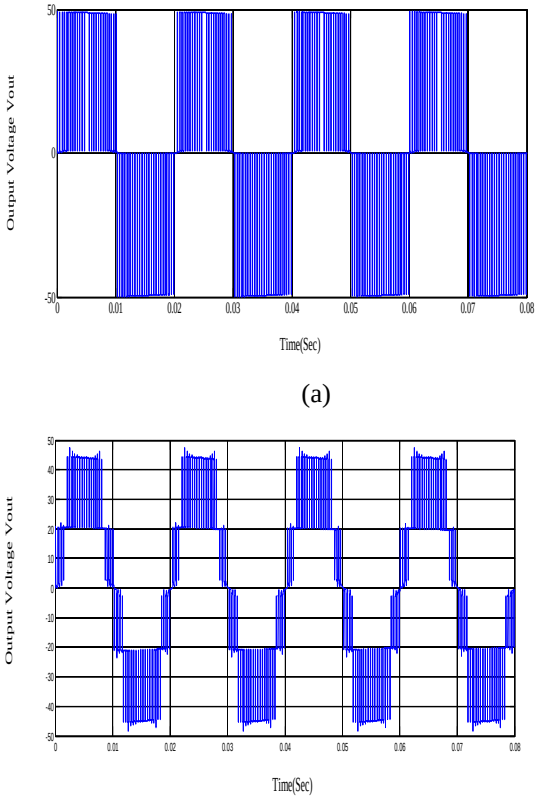

Fig.6. Output voltage waveform V_{out} for (a) three and (b) five level

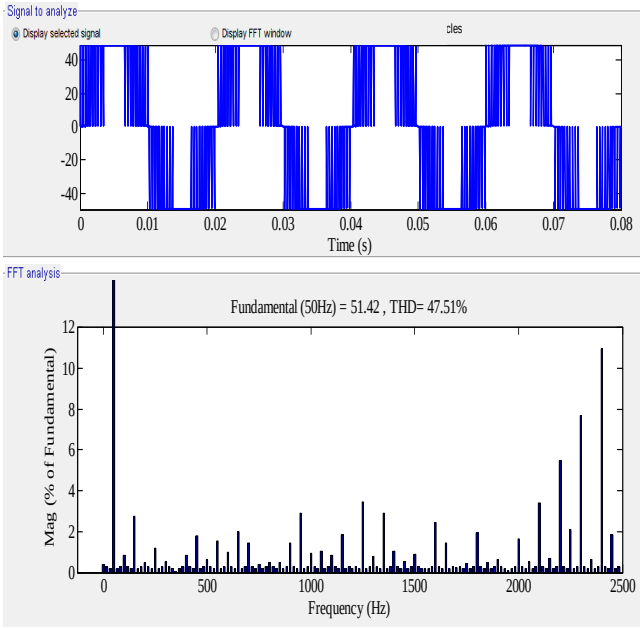

Fig (a), m_a =1.1

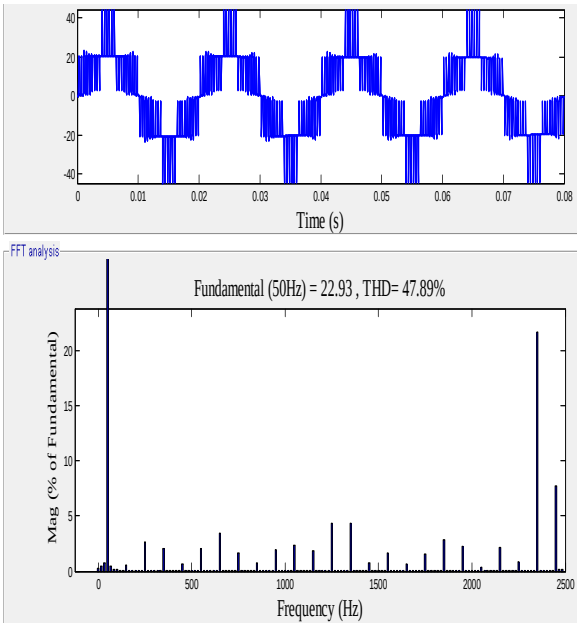

Fig (b) m_a =1.1

Fig.7. FTT analysis for output voltage waveforms Vout (a) three-level, (b) five-level

V. TABLE COMPARISON OF THE CALCULATED THD

Modulation Index	% THD 3-level	% THD 5-level
1.1	47.51	47.89
1	57.93	52.26
0.95	62.08	55.91
0.90	64.71	64.71

VI. CONCLUSION

The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series of capacitors. The concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced. However, with an even number of voltage levels, the neutral point is not accessible, and the term multiple point clamped (MPC) is sometimes applied. Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been limited to three level. Because of industrial developments over the past several years, three levels inverter is now used extensively in industrial application.

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